OPTIMIZATION OF LOW POWER ADDER CELLS USING 90 NM TG TECHNOLOGY

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ABSTRACT: Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits (ICs). Lower power consumption and smaller area are the most important criterion for the fabrication of Digital Signal Processing (DSP) systems and high performance systems like Laptop & Android based applications in order to achieve the best performance with minimized power consumption. In the proposed paper the average power dissipation, transistor count and propagation delay signals have been minimized as the length and width of NMOS and PMOS transistors are optimized. The proposed circuits are designed and optimized using the Transmission Gate (TG) technology, and the comparative performance analysis of these TG based three different 8-bit adders named, Ripple Carry Adder, Carry Look-ahead adder and Carry Bypass Adder has been carried out with 90 nm technology, using TANNER EDA tool.

KEYWORDS: Ripple Carry Adder, Carry Bypass Adder, Carry Look-ahead adder, GPDK 90 nm and TG based CMOS Logic Design Style.

INTRODUCTION

The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of extreme importance. Scaling to deep sub-micron technology, the speed of the circuit increases swiftly. At the same time, the per chip power consumption also increases significantly due to the increasing density of the chip. Consequently, in realizing modern Very Large Scale Integration (VLSI) circuits, low power dissipation and high speed are the two major factors which need to be considered. High performance and low power adders can be designed at different levels such as:

- Architecture - involves the study and designing of the circuits.
- Logic style - illustrates the types of circuit for example ripple carry, carry increment etc.
- Process technology - for example 90 nm, 180 nm, 135 nm technology etc.

As the result, there always exists a trade-off between the design parameters such as speed, area and power consumption. The chief objective of the proposed work is to design an adder circuit with minimum average power dissipation and smaller area as the prime consideration. The most important and widely accepted metric for measuring the quality of the adder designs are the speed, propagation delay and the area. Earlier efforts were more focused towards increasing the speed of computing systems. Reducing power consumption has gained more importance recently because of increasing levels of integration and the desire for portability. Nowadays the demand for portable applications like laptop, personal communication services (PCs) requiring high throughput and vastly increased capabilities is at the peak so as to achieve the wireless connectivity instantly.

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There are three major sources of power consumption in digital CMOS circuits [1] which are summarized in the following equation :-

$$P_{total} = P_{switching} + P_{short\ circuit} + P_{leakage}$$
$$= (\alpha_{0\to1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd}) \quad (1)$$

The first term represents the switching component, where:

- C is the load capacitance
- f_{clk} is the clock frequency
- $\alpha_{0\to1}$ is the transition activity node factor
- I_{sc} is the short circuit current
- $I_{leakage}$ is the leakage current
- V_{dd} is the voltage at drain

The second term is due to the direct path short circuit currents, where I_{sc} , is the short circuit current which arises when both the NMOS and PMOS transistors are simultaneously active, current flowing directly to ground from supply. Finally leakage current ($I_{leakage}$) which can arise from sub threshold effects and substrate injection is mainly determined by fabrication technology considerations. However, the reduction of supply voltage is one of the most effective means to reduce the power consumption, such a reduction requires new design methods for low-voltage and low power integrated circuits. Since an average of 15-20% of the total power is dissipated in glitching and therefore by reducing these glitches of the circuit, low power consumption can be achieved.

LITERATURE SURVEY

M. Alioto and G. Palumbo (2002) compared the main topologies of one-bit full adders on the basis of power consumption, power-delay product (PDP) and speed. Comparative analysis has been done on the two modules of circuit, one with minimum transistor size to minimize power consumption and the other with optimized transistor dimension to minimize power-delay product. Performance has been also compared for different supply voltage values. They showed that except for short chains of blocks or for cases where minimum power consumption was desired, topologies with only pass transistors or transmission gates were not attractive. Then ***S. Panda et. al. (2009)*** stated that the full adder was built by 28 transistors revealing a very high transistor count. The average and leakage power consumption as well as delay is very high. In this paper a novel circuit is made mainly by the TG technology through which they used only 18 transistors to implement the Boolean expression of the full adder. So, by making the advanced full adder circuit they reduced the transistor count and reduced the power consumption and delay of the circuit. Further ***S. Wairya et. al. (2010)*** presented a novel design full adder circuit based on XOR- XNOR design in a single unit. Investigation of the power, delay and power delay product (PDP) of low voltage full adder cells in different CMOS logic styles was done. Simulation results illustrated the superiority of the proposed adder circuits against the conventional CMOS, XOR-XNOR, Hybrid and Bridge adders' circuits in the terms of power, delay and PDP. The performance of the full adder circuits is based on GPDK 90 nm CMOS process models at supply voltages starting from 0.65 V to 1.5 V evaluated and compared of the simulation results obtained from Cadence. Later ***R. UMA et. al. (2012),*** presented the selection of the adder topology with tradeoff between power consumption, area and delay. The adder topologies used in this work are carry look- ahead adder, ripple carry adder, carry skip adder, carry select adder, carry save adder, carry bypass adder and

carry increment adder. The performance issues like power dissipation, area and delay are analyzed using Micro wind tool.

MOTIVATION

Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of the ICs. Lower power consumption and smaller area are the most important criterion for the fabrication of Digital Signal Processing (DSP) systems and high performance systems like Laptop & Android based applications in order to achieve the best performance with minimized power consumption. The conventional CMOS full adder was built by 28 transistors revealing a very high transistor count. The average as well as leakage power consumption and delay are very high. In order to achieve an improvement in these performance parameters, TG technology using 90 nm has been proposed.

PROPOSED WORK

The increasing demand for portable devices and hand held equipments gives the low power design techniques more consideration. Therefore, the average power consumption and signal propagation delay are critical to the design of high performance very large scale integration circuits. The main objective of the proposed work is to minimize the Average Power Dissipation, Transistor Count and Propagation Delay as the length and width of NMOS and PMOS have been optimized. The proposed circuits are prototyped and optimized using the Transmission Gate (TG) technology, and the comparative performance analysis of TG based 8-bit adders has been carried out with 90 nm technology, using TANNER EDA tool.

SOLUTIONS AND METHODOLOGY

The minimization of the Average power consumption, transistor count and propagation delay are the major objectives intended for designing the adders named as Ripple carry adder (RCA), Carry look-ahead adder (CLA) and Carry bypass adder (CBA) . Hence, by optimizing the parameters and with the application of algorithms led to realize the obligatory simulation waveforms.

Algorithm used

- Select the 90 nm technology.
- State the desired transient range of the waveforms preferred to be displayed.
- Cite all the specified inputs as well as the outputs of the prototyped circuit.
- Compute the average power consumption by stating the coinciding point of V_{dd} and ground.
- Evaluating the signal delay by assigning a precise trigger and target value.

Parameter tuning

Using the 90 nm technology, the channel length of all the desired circuits is fixed i.e. 0.09 μm as the typical reference value.
Now, in order to finalize the values for the channel widths of both NMOS and PMOS transistors we calculate β, where:
β = (channel length / 2)
Hence β = (0.09 / 2) = 0.045 μm
$\boldsymbol{W_{NMOS}}$ = 3 × β and $\boldsymbol{W_{PMOS}}$ = 3× $\boldsymbol{W_{NMOS}}$

= 3 × 0.045
= 3 × 0.14
= 0.14 µm
= 0.42 µm

As the above evaluated values of channel length and width of NMOS and PMOS transistors, as the starting limit and varying the widths of NMOS and PMOS transistors within a specific range of

0.14 µm ≤ W_{NMOS} ≤ 0.42 µm and 0.42 µm ≤ W_{PMOS} ≤ 1.3 µm

Therefore, by varying W_{NMOS} and W_{PMOS} within the above assigned limits, the final optimized parameters are obtained which corresponds to the best results with minimized power dissipation and propagation delay.

Optimized parameters (for all 8-bit Adder Circuits):-

- Channel Length = 0.09 µm
- Width of NMOS = 0.35 µm
- Width of PMOS = 1.0 µm
- With referenced voltage V_{dd} = 1.2 V

RESULTS AND SENSITIVITY ANALYSIS

The result of Table I shown below is carried out by using specified gate widths of NMOS & PMOS and a minimum length of 0.09 µm for NMOS and PMOS. The result is carried out at 1.8 V supply voltage and average powers consumed and delay at sum and carry output are finding out.

Table 1: Performance Parameters of 8-bit Adders

Software Used	Adder Type	Transistor Count	Avg. Power Dissipation (mw)	Propagation Delay at Carry (ns)
TANNER EDA Tool (using 90 nm)	RCA	146	0.032	0.035
	CLA	240	0.073	0.016
	CBA	240	0.071	0.042

Two aspects are important for adder design: the Average Power Consumption and delay of sum and carry operation. The simulations for these two aspects for different 8 bit adders are obtained in TANNER tool in the following section. Waveforms of the Ripple carry adder are shown in the Fig. 1 with three inputs such as a, b and c and two outputs names sum and carry.

Similarly, the simulation results have been depicted in the following Fig. 2 and Fig. 3 showing the waveforms of the Carry look-ahead and Carry bypass adder respectively with a, b and c as inputs and sum and carry as the outputs.

DATA MODEL (SCHEMATICS)

Schematic of different adders are shown in Fig. 4, Fig. 5 and Fig. 6 having three inputs A, B, C and two outputs sum and carry. In these prototypes, all simulations are run using Micron Technology's 0.09 µm process which models with typical n-channel and p-channel drive at 1.8 V

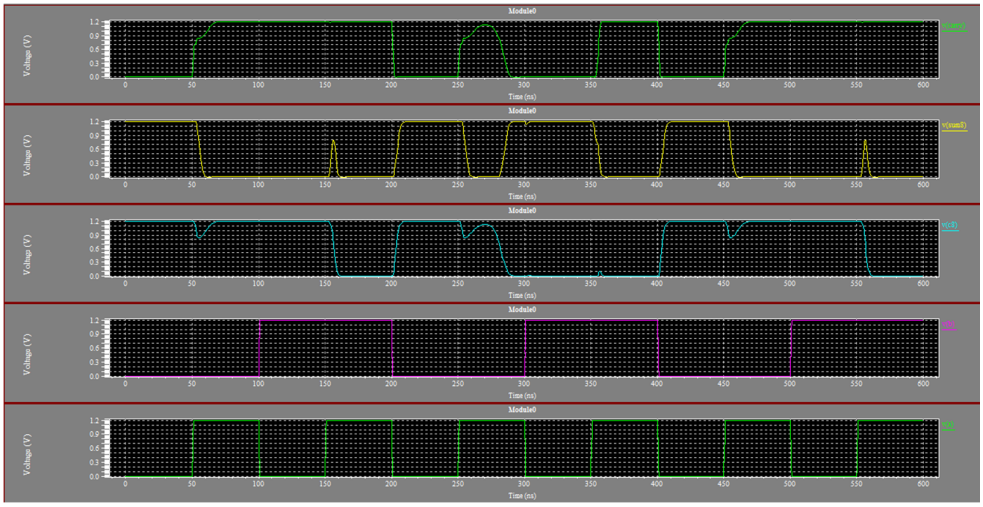

Figure 1: Waveforms of Ripple Carry Adder

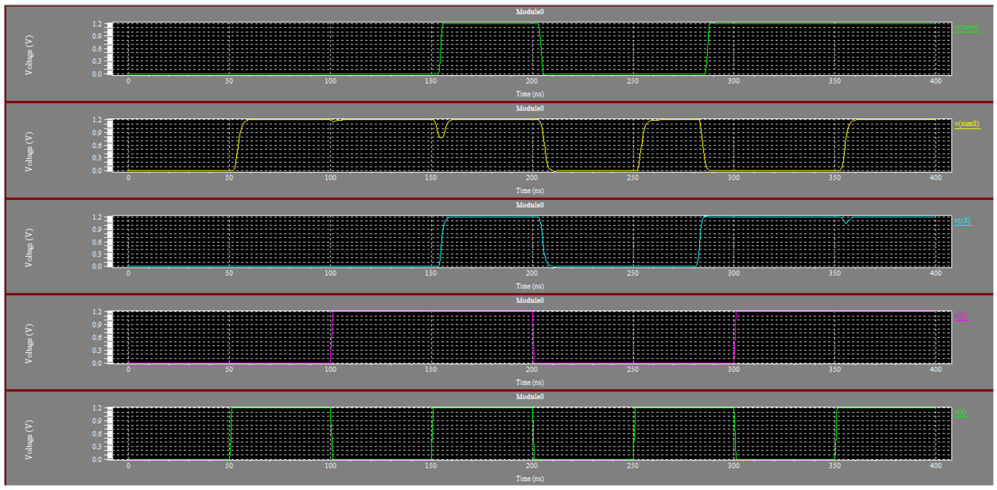

Figure 2: Waveforms of Carry Look-ahead Adder

power supply. In the schematics all logics are designed using different values of gate width of and a minimum length of 0.09 µm for both NMOS and PMOS.

Schematic of a Ripple carry adder is shown in the following Fig. 4, comprising XOR and Multiplexer gate thus resulting into the desired outputs.

Similarly, the schematic data models of Carry look-ahead adder and Carry bypass adder is shown below in the Fig. 5. and Fig. 6, comprising XOR, MUX , AND and OR gates.

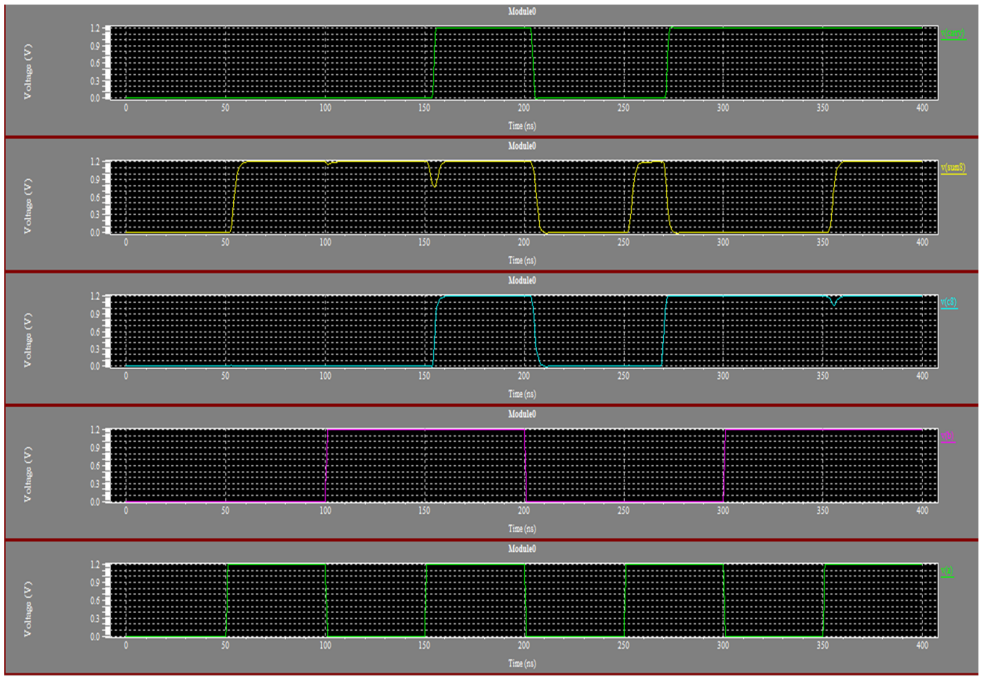

Figure 3: Waveforms of Carry Bypass Adder

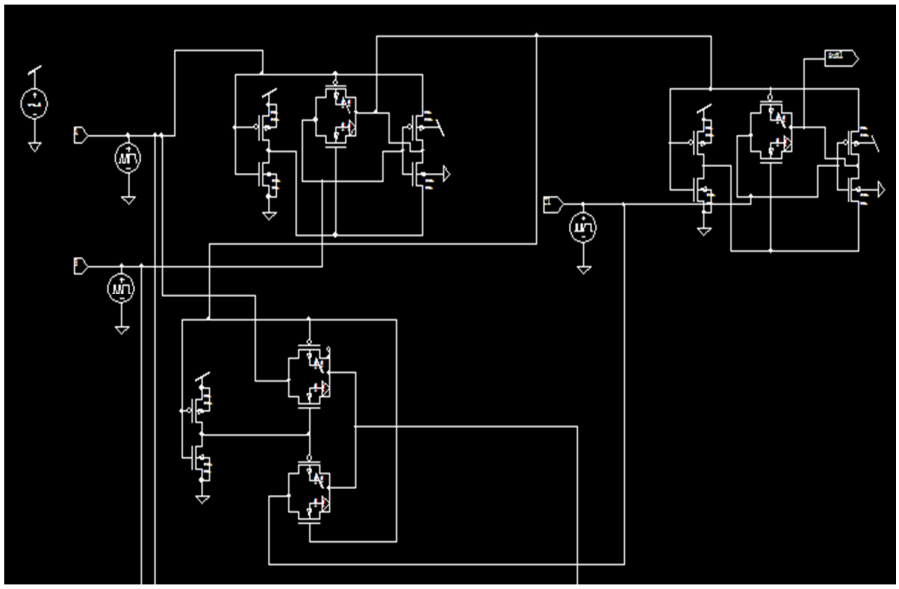

Figure 4: Ripple Carry Adder using TG Technology

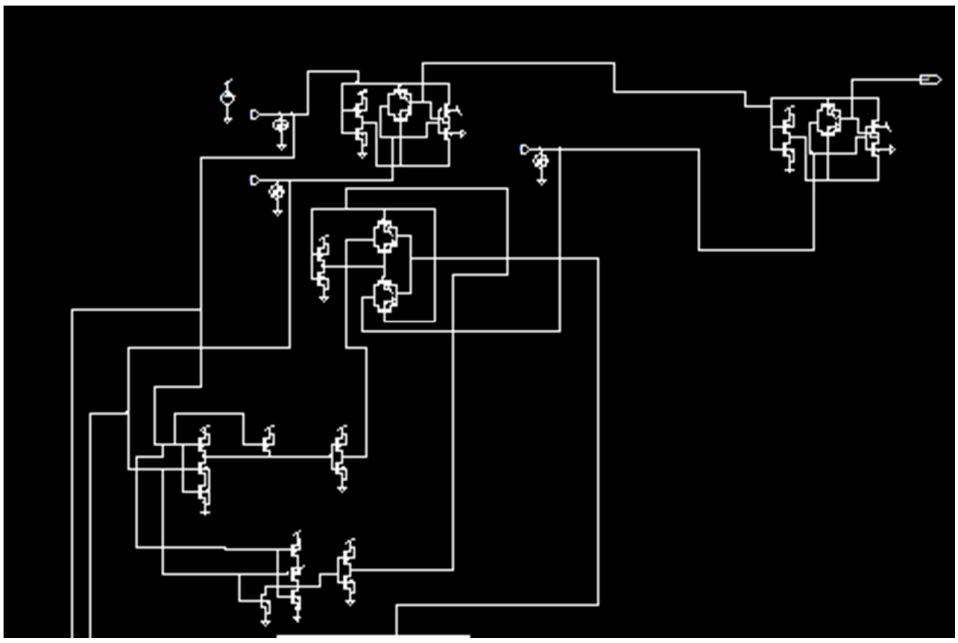

Figure 5: Carry look-ahead Adder using TG Technology

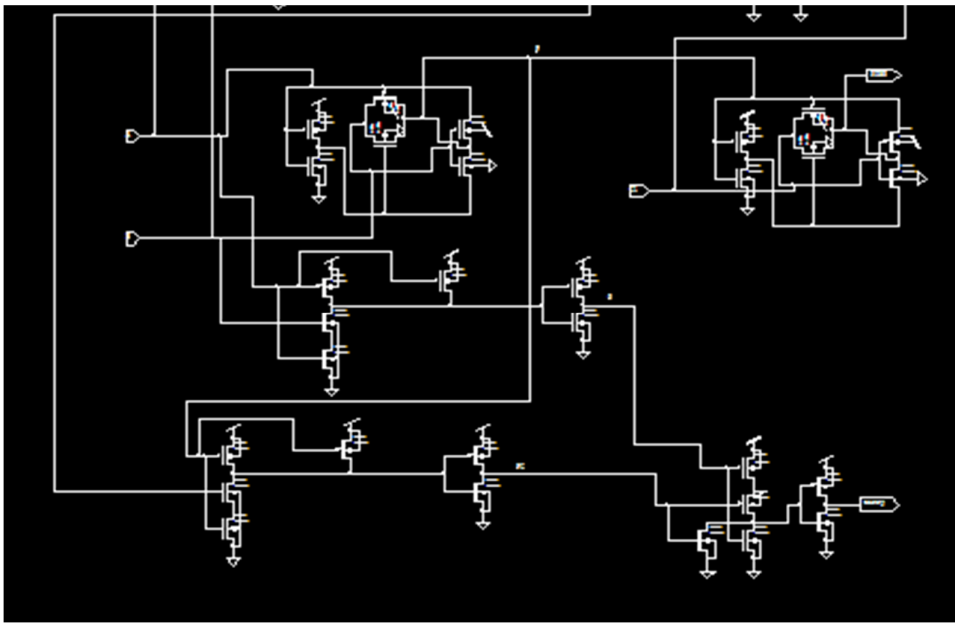

Figure 6: Carry Bypass Adder using TG Technology

COMPARISON OF RESULTS

The comparative performance analysis of three different 8- bit adders is shown below in the following Table 2, Table 3 and Table 4.

Table 2: Comparative Analysis of Performance Parameters of 8- bit Ripple Carry Adder

Algorithm Type	**Software Used**	**Ripple Carry Adder**		
		Transistor Count	**Avg. Power Dissipation (mW)**	**Propagation Delay at Carry (ns)**
R.UMA et al. [5]	MICROWIND TOOL	288	0.206	4.208
N. JAURA et al. [9]	TANNER EDA TOOL	146	0.041	0.016
Proposed Algorithm	TANNER EDA TOOL	146	0.032	0.035

Table 3: Comparative Analysis of Performance Parameters of 8-bit Carry Look-ahead Adder

Algorithm Type	**Software Used**	**Carry Look-ahead Adder**		
		Transistor Count	**Avg. Power Dissipation (mW)**	**Propagation Delay at Carry (ns)**
R.UMA et al. [5]	MICROWIND TOOL	272	0.312	3.1
N. JAURA et al. [9]	TANNER EDA TOOL	240	0.089	0.016
Proposed Algorithm	TANNER EDA TOOL	240	0.073	0.016

Table 4 Comparative Analysis of Performance Parameters of 8-bit Carry Bypass Adder

Algorithm Type	**Software Used**	**Carry Bypass Adder**		
		Transistor Count	**Avg. Power Dissipation (mW)**	**Propagation Delay at Carry (ns)**
R.UMA et al. [5]	MICROWIND TOOL	372	0.459	3.01
N. JAURA et al. [9]	TANNER EDA TOOL	240	0.086	0.015
Proposed Algorithm	TANNER EDA TOOL	240	0.071	0.042

CONCLUSION

In the proposed work, the comparative performance analysis of the 8- bit full adder circuits with 90 nm TG technology has been carried out. The comparative performance analysis has been done on propagation delay, average power dissipation and transistor count. The performance analysis, comparison and waveforms depicting simulation results have been depicted in the above shown Tables and Figures and the achieved results reveal that there is a huge decrease in the average power dissipation in the three proposed circuits. Similarly, the performance parameters in case of all the 8- bit full adders i.e. RCA, CLA and CBA using 180 nm and 90 nm technologies when compared with the results shown by R. UMA et. al. [5], reveals that there is an enormous reduction in all the three parameters i.e. transistor count, average power dissipation and propagation delay. Thus, the results indicate that CBA is the fastest full adder topology with minimum propagation delay even with maximum transistor count amid RCA, CLA and CBA.

Hereby it is concluded that average power dissipation and propagation delay in TG based adders are very less as compared to conventional CMOS and other circuits. As a result, it is concluded that RCA requires the minimum power because of minimum number of transistors used in the designed circuit. Although the propagation delay of RCA is approximately comparable with CLA and CBA, along with minimum Average Power Dissipation RCA is the best amongst all.

FUTURE SCOPE

TG based advanced full adder circuits, reduces the transistor count, average power dissipation and propagation delay of the circuit. This proposed work may be further extended by various ways as:

- The work can be extended to higher bit adders.
- The research can be further extended to optimize the parameters via frequency, capacitance, length, width etc.
- The work can be even extended to vary the technology file.
- The efforts can be made to reduce the transistor count which further leads to reduce the average power dissipation, area and the propagation delay by changing the various parameters.
- Further the research steps can be utilized by using the other types of adders like Carry Select Adder, Hybrid adder, Carry Skip Adder, Carry Increment Adder etc.

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